Impact of Voltage Transients and System Impedance Ratio on Zone 1 Distance Relay Reach

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Abstract— Capacitive voltage transformers (CVT) are a cost-effective solution to provide voltage signals for high-voltage transmission line protection. While cost-effective, these devices do also come with limitation that may be problematic to distance protection, especially underreaching Zone, Zone-1, in certain applications. CVTs have stored energy that when subjected to sudden primary voltage changes can produce transients in the secondary circuit connected the transmission line protection. These transients depend on the design parameters of CVTs such as capacitance values, type of ferro-resonance circuits installed on the secondary winding, and also on the loading of the CVT. Voltage available to the relay during faults on the line also depends on the source impedance to line impedance ratio, SIR. The higher the ratio of SIR, lower will be the voltage at the relay for line end faults. CVT transients may dominate during the transient period lasting for a cycle or two and if measurements and decisions are made within this transient period, they are prone to errors. The paper discusses the impact of CVT transients and high SIR on zone 1 distance element, discusses available industry standards to specify CVTs with faster response and relay designs to reduce overreach issues. Finally, simulation results with SIRs up to 40 and actual field events are presented.

***Index Terms*— Capacitive Voltage Transformers, SIR, CVT Transients, Distance relay, zone-1 overreach**

INTRODUCTION

Distance relays have been used as main protection scheme for protecting transmission lines for a long time. These are impedance measuring units with voltage and current inputs provided by instrument transformers, voltage transformers and current transformers, which scale down the primary values to the relay input levels of 115V and 5A under normal fully loaded lines. The accuracy of measurement depends on the accuracy of input three phase voltages and currents. The relay is programmed to operate if the calculated impedance is less than the set point called the reach. The instantaneous distance element is set to underreach the length of the line by a margin of 15% to 20% and is termed zone 1. Accuracy of measurement depends on the accuracy of instrument transformers and tolerance and calculation accuracies within the relay. Voltage magnitude available to the relay during faults on the line also has an impact. Following clauses analyze each of these parameters.

I. SYSTEM IMPEDANCE RATIO

Source to line impedance ratio, SIR, also known as the system impedance ratio, is defined as the ratio of the source impedance behind the relay location, Z_S to the line impedance protected by the distance relay, Z_L. SIR $=\frac{ZS}{ZL}$

Referring to Figure-1, for a fault at the end of the relay reach, Z_L, the voltage at the relay location,

$$V_R = \frac{E}{(ZS+ZL)} * ZL = = \frac{E}{\left(\frac{ZS}{ZL}+1\right)} = \frac{E}{(SIR+1)}$$

where, E is the phase to ground voltage.

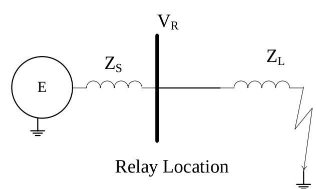

Figure-1: System one-line

As the source impedance increases or as the system gets weaker, the voltage at the relay location decreases for a fault at the same location. The voltage equation provided above is valid for three phase faults and phase to phase faults with the source and line impedance values corresponding to the positive sequence parameters. For single line to ground faults, GE "Protection& Automation Application Guide" [1] provides the following equations to determine the voltage at the relay location:

$$V_R = \frac{E}{\left(\frac{Z_S}{Z_L}\right) * [\frac{(2+p)}{(2+q)} + 1]}$$

where, $Z_S = 2Z_{S1}+Z_{S0} = Z_{S1}(2+p)$; $p = \frac{Z_{S0}}{ZS1}$

and $Z_L = 2Z_{L1}+Z_{L0} = Z_{L1}(2+q)$; $q = \frac{Z_{L0}}{ZL1}$.

IEEE transmission line protection guide, C37.112 [2] provides a detailed approach to calculate the SIR for various faults. Though these equations provide methods to determine the available voltage for a line end fault, it is a tedious task to go through these methods. A much simpler approach is to make use of the information available from the fault programs where the system is modeled and the voltage, V_R, at the relay location for a fault at the zone reach can be determined for various types of faults. The worst case with contingencies that provide the

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lowest voltage for faults is determined. SIR can be easily calculated by the equation, SIR $=[\frac{E}{VR} - 1]$ (1)

Distance Relay designs and voltage sensitivity influence the accuracy of the measurement at the reach point especially when the available voltage to the relay is low due to high SIR. Operating times of electro-mechanical and few static designs increased due to decrease in voltage magnitude as the fault location was moved closer to the reach. This had inherent advantage of allowing any voltage transients to die down as the faults were closer to the reach. Typical operating times were provided either as constant time contour curves for various values of SIRs or as typical operating times at various fault locations for a specified SIR as shown in
Figures-2a and 2b.

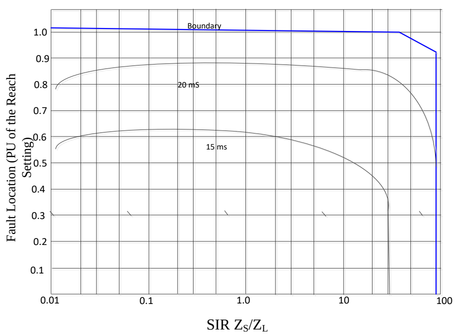


Figure-2a: Constant time contours

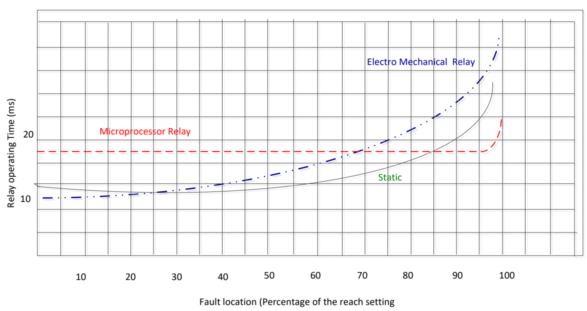


Figure-2b: Typical Relay Operating times based on Fault location at a specific SIR *

*- These curves are redrawn from GE -PAAG book

II. Impact of SIR on Distance Relay operating quantity (IZ-V)

Operating principle of distance element can be easily summarized as comparing the phase relationship between an operating quantity (IZ-V) with a reference voltage, V_P to generate Mho Characteristics. Changing the reference voltage to a current based quantity will generate quadrilateral characteristics.

In the operating quantity, Z is the relay reach and I and V are the currents and voltages from faulted phase(s). These quantities vary depending on the fault type. For single line to ground (A-G) fault, the current is the compensated current ($I_A+K_0I_N$) and voltage is V_A, where K_0 is the zero-sequence compensation factor. The polarizing quantity can be the pre-fault or the positive sequence memory voltage. For phase to phase (B-C) fault, the current used is (I_B-I_C) and voltage used is (V_B-V_C).

If we examine the sign of the compensated Voltage term, (IZ-V), it will be zero for a fault at the reach, will be positive if the fault is within the reach and negative if it is beyond the reach as illustrated in the figure-3.

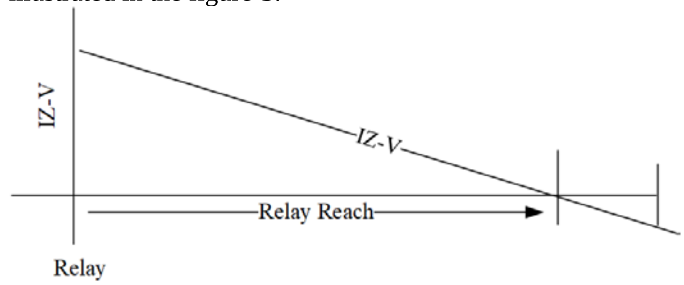


Figure-3: Plot of compensated voltage, (IZ-V) for various locations of the fault up to and beyond the reach.

(IZ-V) at any location 'M' on the line with an impedance of 'MZ' is given by (IZ-V) = $\frac{(1-M)}{(SIR+1)}E$

Figure- 4 shows how the slope of (IZ-V) decreases with increase in SIR.

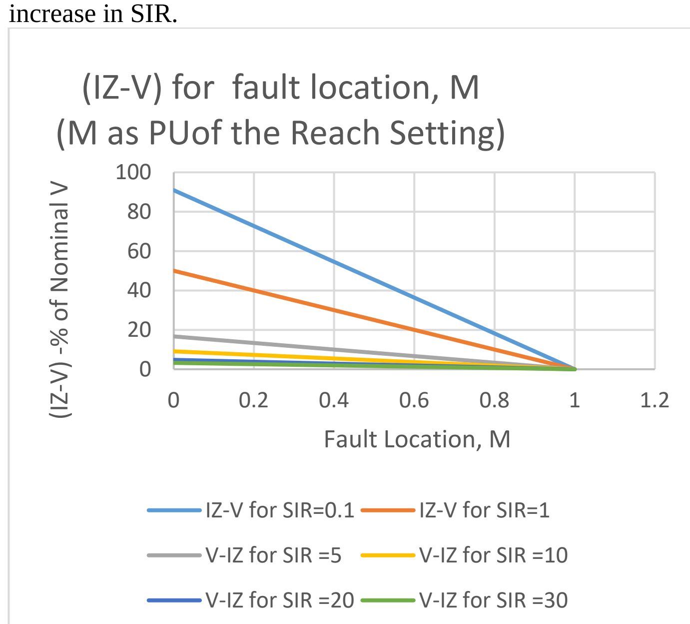


Figure-4: (IZ-V) variation with fault location at different SIR

Inaccuracies in current and voltage measurements and the errors in impedance setting will result in change in the (IZ-V) polarity resulting in overreach or underreach of the distance element. With the Zone 1 element in a distance scheme set to 80% of the protected line section, 20% margin is assumed to be safe enough to prevent operation of this zone element for faults beyond the protected line section. (IZ-V) at 20% below the reach as tabulated in Table-1, provides an indication of the limit on errors to prevent overreaching of zone 1 for faults beyond the protected line section.

SIR	0.1	1	5	10	20	30
%(IZ-V)	18.2%	10%	3.3%	1.8%	0.95%	0.65%

Table-1 Percentage Change in (IZ-V) at 80% of the reach setting.

If errors in measurement exceed numbers in Table-1, zone 1 operates for faults beyond the line section. From Table-1, we can infer that the reach may need to be pulled back to get better margin at higher SIRs.

III. Factors contributing to errors in (IZ-V) computation

Assuming additive errors in current and voltage measurements and in impedance setting, cumulative error can be calculated for a specific application to determine the maximum settable reach. General discussions on the accuracy calculations are provided in the subsequent paragraphs.

C-Class current transformers are generally used, and these have 3% error at the rated current and maximum 10% error at twenty times the rated current at the rated burden. Typical steady state errors of Impedance, Z, setting is 3% and may increase at higher SIRs. Assuming 5% error in the line impedance parameter calculations, errors introduced by the impedance can be as high as 8%. It is to be noted that the current may not be as high as twenty times the nominal at higher SIRs and with burdens much lower than the rated burden, CT steady state accuracy will be very high. The secondary current in a CT will be lower than expected as a portion of the current will be used up as excitation current depending on the burden. During faults, currents may have DC offsets and modern relays with mimic filters successfully reduce the impact of DC. With saturated currents, relay tend to measure lower current magnitudes resulting in underreaching of distance elements. CT saturation will not result in zone-1 overreach. Error introduced by CT is assumed to be 5% for our discussion.

IZ term worst case cumulative value would then be
1.05*1.08*IZ =1.134*IZ which has an error of 13.4%.

Voltage Transformers, wound type as well as capacitive voltage transformers have voltage steady state accuracies specified from 90% to 110% of the nominal voltage as per IEEE standard C57.13 [3]. Accuracy class can be specified either at 0.3%, 0.6% or 1.2%. IEC 61869-5 [4] also specifies errors for CVTs from 5% to 100% of the nominal voltage and provides an additional error at 2% voltage which would be twice the error allowed at higher voltages. As an example, a 0.3% accuracy class CVT will have error not exceeding 0.6% at 2% of the rated voltage. This error is always defined one cycle after the fault incidence.

Wound type voltage transformers, due to low capacitance, will accurately stepdown the primary voltage without any transient errors. If wound PT is used, worst-case error in (IZ-V) can be as high as (13.4+0.3) = 14%. If we assume that the errors contributed by wound PT may not impact significantly, the zone 1 overreach with 15-20% setting margin would be adequate.

IV. CVT design Considerations

A high-level component list for a capacitive voltage transformers (CVT) consist of a capacitive voltage divider with a phase angle tuning reactor, a step-down transformer, and a ferro-resonance suppression circuit as shown in figure-5. The CVT functions by reducing the primary voltage of the system to an intermediate voltage level before it is further reduced by the step-down transformer to a level acceptable for the protective relaying. The phase angle tuning reactor's purpose is to cancel the reactance effect of the capacitance in voltage divider, keeping the secondary voltages at the same phase angle that of the power system. Finally, the ferro-resonance suppression circuit is required to dampen any resonance between the step-down transformer's iron core and the capacitance in the circuit.

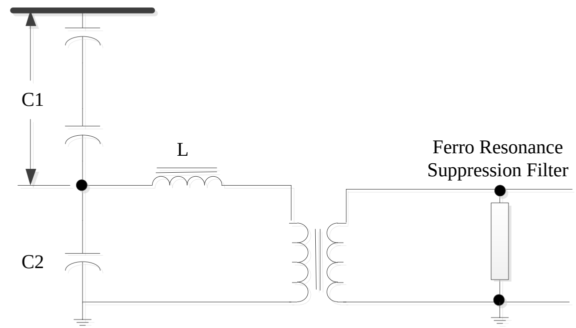


Figure-5: Simple CVT Model

Ferro-resonance suppression filters are of two types, active and passive filters as shown in figure-6.

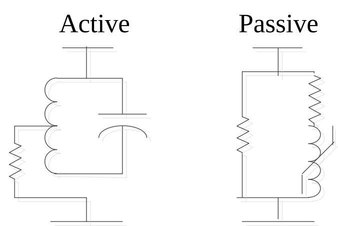


Figure-6: Ferro-Resonance suppression Circuits

Active filter comprises of an L-C tank circuit tuned to 60 Hz whereas a passive filter has a saturable reactor in series with low resistance that provides damping if voltage exceeds 150% of the nominal. Active filters add to oscillations when the primary voltage is suddenly reduced. Though the CVTs bought today are only with passive suppression filter, many CVTs with active filters are still in service on the power system today.

When choosing a CVT for a protective relay purpose there are only a few options to help mitigate the transient effects for a sudden voltage changes at the primary level. Regardless of these options, all CVTs will have some level of transient response with greatest amount seen for faults occurring at a voltage zero and with a large system voltage drops. As per IEC standard, transient response errors of CVTs are specified at one cycle after the fault. The error is specified as not to exceed 10% of the final value. CVT manufacturers can also provide CVTs with a tolerance of 5% after one cycle but is expensive due to the use of high capacitance and larger transformer size. As mentioned earlier, IEC standard also specifies the allowable error at 2% of the rated voltage which corresponds to SIR of 49 as per equation (1). For a 0.3 class CVT, maximum error would be 0.6% at 2% of the voltage. IEC document has a special class of CVTs defined as Class T3 where the errors are limited to 4% of the final value after half a cycle and 2% of the final value after one cycle. These designs require a special damping device. IEC standard also states that *"If a damping device is used, the proof of the reliability of this device should be part of an agreement between manufacturer and purchaser"*. Several papers have been published over the last fifty years and few notable ones are listed as the references [5] through [8].

Response of one type of CVT is as shown in figure-7.

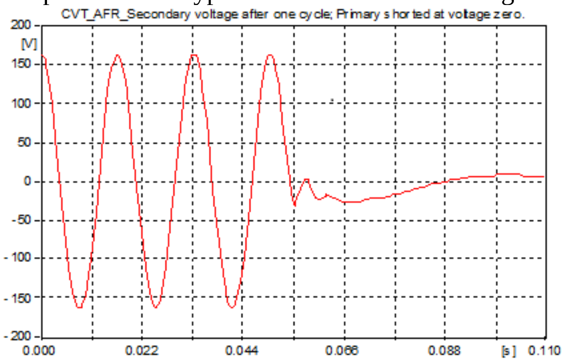


Figure-7: Transient Response of CVT

CVT transients can be oscillatory-periodic or aperiodic. Higher capacitance designs tend to provide a decaying (aperiodic) transients and normal capacitance generate periodic decaying transients with frequencies close to the power frequency which are not filtered out in digital relays. Details of the designs are discussed in reference paper [6].

CVT errors also depend on the loading of the CVT. Lighter loading as with only digital relays connected to CVTs, tend to generate less peak transient than with heavily loaded CVTs as mentioned in [6],[7] and [8]. Actual test reports from the manufacturer supplying the CVT is the best way to verify these statements.

With the use of CVTs on relays with faster operating speeds at the zone reach, majority of errors in (IZ-V) seem to originate from the CVT transients. Depending on the type of CVT used and on the operating time of the relay, errors introduced in (IZ-V) may result in out of zone operation for line end faults. If relay operating times are inherently slower at the reach point, transient overreach issues are not encountered whereas if relay operating times are almost constant and closer to one cycle, there is a tendency for overreach unless special measures are incorporated in the relay design.

V. DESIGN LOGIC IMPLEMENTED IN MODERN RELAYS TO PREVENT ZONE 1 OVERREACH:

One of the solutions is to reduce the reach of zone 1 to improve allowable error tolerance. But, in some cases, zone-1 reach may need to be pulled back to such an extent that it may protect only a small portion of the line. Such a pullback may also be needed if the relay is operating at sub-cycle speed. Delaying the operation of zone-1 to allow decay of transients seems to be a good method but, it introduces permanent delay even for a close-in fault. Relay manufacturers have implemented methods to determine such a situation of low voltage for faults with high SIR in deciding to add appropriate delays [6],[8]. Voltage threshold, both for phase to ground and phase to phase voltages, are used along with current thresholds to determine the high SIR condition resulting in delaying the zone 1 operation. In addition, if the impedance calculation is not steady but jumping in and out of the tripping characteristics, the decision is delayed preventing operation. In another design, an internal zone, with pulled back reach based on zone 1 setting, is implemented to operate without any delay if the voltage input to the relay is below a threshold voltage in addition to instability of impedance calculation [6].

VI. RELAY PROTECTION DESIGN- SIGNAL TO NOISE RATIO

Historically, many utilities have always used the 67V taps on CVTs and PTs for line protection needs, while synchronizing relays/elements and meters used the 115V tap. This practice was cemented in the protection practices due to relay voltage input limitations on older electromechanical relays. Today, protective relays are microprocessors which no longer have this low-level voltage input limitation. The general acceptable input voltages for these modern-day relays have an upper limit above 250V. By utilizing this higher limit, a single voltage tap from the voltage instrument transformers could be used for all protective, synchronizing, and control needs in the substation. This change has cost savings benefits in construction. More importantly, using the high voltage tap from the instrument transformers does give 'better' voltage sensitivity for microprocessor line relays. The use of full tap also increases the signal to noise ratio of the relay terminal voltage by 1.73 (assumes CVT with 115V/66.4V taps). As an example, for a line with SIR of 20, for end zone fault, the voltage at the relay would be 0.048 PU. With 66.4V tap, the actual voltage would be 3.16 V whereas with full tap it would be 5.48V providing a better signal to noise ratio.

VII. SIMULATION RESULTS

230 kV, 2-mile line was modeled that is connected to an infinite system as shown in the one-line as in figure-8

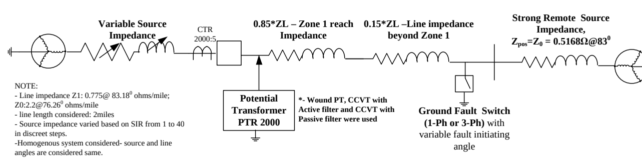


Figure-8: One Line model of the System simulated in PSCAD

The source impedance behind the relay location was varied to provide SIR from 1 to 40 in steps of 5. Zone 1 phase and ground distance elements were set to 85% and 125% of the line impedance. Voltage transformer secondaries were rated for tapped voltage. Voltage transformer secondaries were not loaded with additional resistors.

Single line to ground fault and three phase faults were simulated at the end of the line. Fault incidence angles were varied from 0^0 to 150^0 for each SIR value for both three phase single line to ground faults. These tests were repeated with a wound PT (modeled as an ideal PT), CVT with active filter and CVT with passive filter. Models of CVTs were obtained from manufacturers. CTs were also modeled with no magnetic

saturation. Several relays from two manufacturers (six relays in total) were tested and there was no misoperation observed on any relays till SIR of 30. It is to be mentioned that only the relay operation was monitored and not all captured COMTRADE files were not analyzed to reduce the duration of the analysis.
Zone-1 overreached for line end faults in most of the relays with either transient detection logic disabled or with no zone-1time delay in simulation cases with Active FR suppression CVTs. All of them operated when fault was initiated closer to voltage zero crossing. One simulation case (three phase fault) at SIR of 40 and with CVT with active ferro-resonance suppression filter, relay momentarily picked up. The fault incidence angle was at A-phase voltage zero as shown in Figure-9

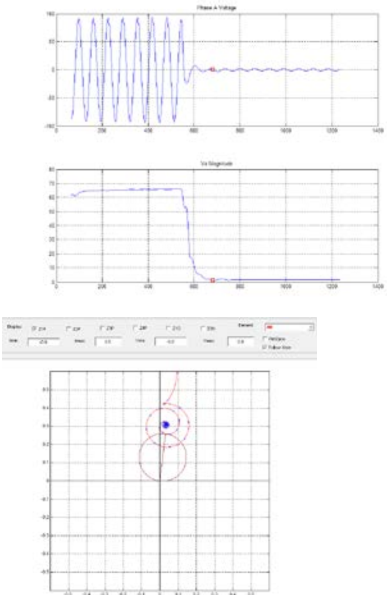


Figure -9: Voltage waveform and impedance Trajectory for three -phase fault with fault initiation at A-phase voltage zero and CVT with active ferro-resonance suppression filter.

Additional time delay on zone1 prevented relay operation for end line faults.

While few simulated cases studied had Zone 1 overreach due to CVT transients for line end faults, many cases showed the transient impedance trajectory swinging into the zone-1 mho momentarily while decaying. This can be seen in the relay's records illustrated below in figure 10. In this lab simulated case the zone-1 reach was set at 85%, SIR at 40, and there was no added zone-1 delay. The observed transient impedance trajectory would be inside the zone-1 mho for roughly a quarter cycle or less before swinging out again. The impedance relay did not operate due to the relay requiring multiple samples showing the fault impedance inside the mho. However, with the relay reach was set to 85% an overreach occurred. Following actions prevented the relay from overreaching:

- Addition of a 1 cycle delay on the zone-1 elements
- Pulling back the reach to 80% or less for SIRs at or above 30
- Prevent operation by enabling transient detection logic in the relay.

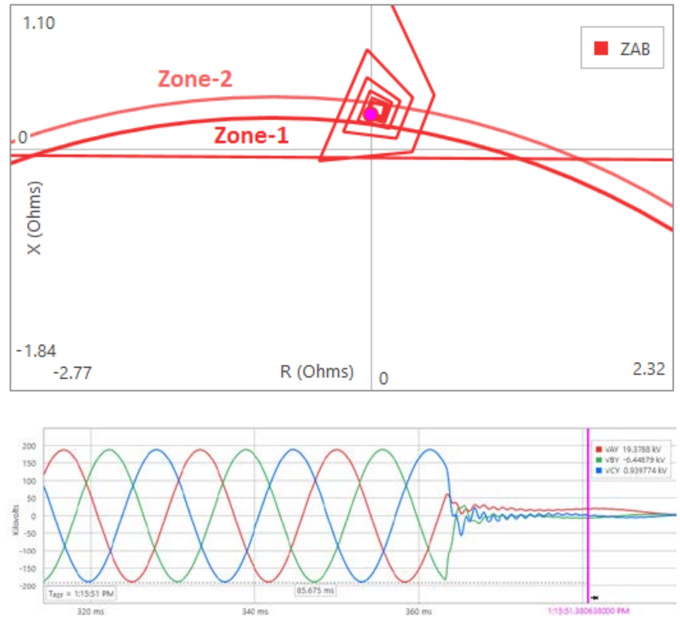


Figure-10: Impedance Trajectory during three phase fault and voltage waveforms

In a separate simulated SLG case with zone-1 ground distance elements set at 60%, a transient over operation was observed. In this case the tested SIR was 40 and there was no zone-1 element delay (or transient protections enabled). This case (Figure-11) is notable and illustrates the inherent delay on the zone elements in the microprocessors for a large transient condition. The zone-2 ground element picks up in roughly 25ms after the initiation of the fault. Zone-1 element picks up 8.25ms after the zone-2 ground element and gives a trip condition for roughly 6.5ms before dropping out. one cycle delay prevented tripping due to transient overreach.

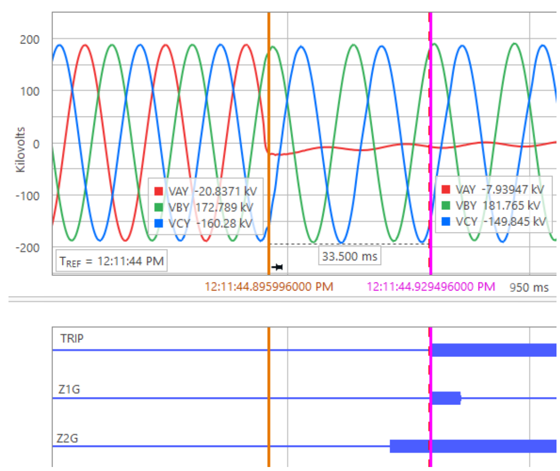
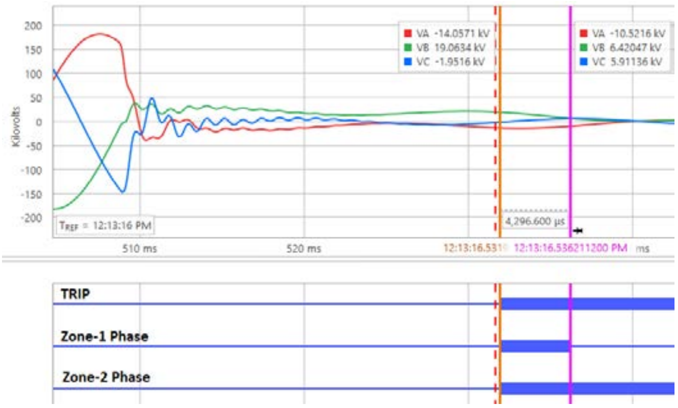


Figure-11: Zone-1 pulsed two cycles after the fault

In the lab simulations, Zone-1 overreaches were observed in cases of SIR as low as 30. As with the cases with SIR of 40, zone-1 elements pickup up for less than a 1/2 cycle. In the case illustrated below (Figure-12), the zone-1 phase element operated for a 3-phase remote end fault with an SIR of 30. The Zone-1 element picked up roughly 22.5ms after the fault initiation and remained picked up for roughly 4.2ms. In this case no delay was set on the zone-1 element or any transient detection logic in the relay was enabled in the relay.



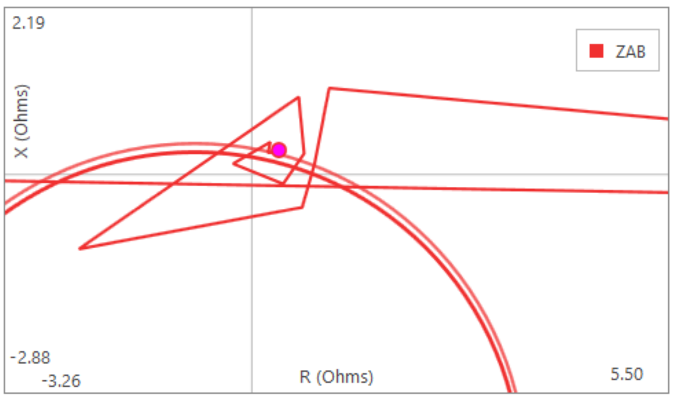


Figure-12: Zone-1 overreach for three phase faults: SIR-30

The simulation model did not load CVT secondary. Discussions of loading is well covered in references [6] and [7] where statements are made that lightly loaded CVT generate less transient peak but takes longer to dissipate whereas fully loaded CVT dissipates energy faster. As mentioned earlier, the best way to determine the CVT response is to obtain test plots from the manufacturer. Probably, increasing loading might have prevented delayed zone 1 response but these cases were not simulated.

VIII. Actual Events resulting in overreach due to transients

Case Study-1:345 kV single line to ground fault at the remote end:

At a 345 KV substation, internal flashing in an open breaker resulted in creating a B-Phase to ground fault.

At one of the remote ends of a 21.4-mile line connected to this faulted station, zone-1 ground element over tripped despite the reach set at 80% of the line's impedance. The voltage input was from an active CVT. Event records show that the fault's impedance trajectory at its initiation swung into the ground zone-1 mho for less than a ¼ cycle and quickly exited. Roughly 1 cycle after the fault initiation the fault impedance trajectory was around 98.9% (12.82 Ω_{pri}) of the line's impedance.

This can be seen below in the event report's mho impedance illustration below as in figure-13 and Figure- 14

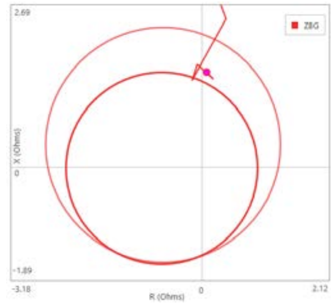


Figure-13: Impedance Trajectory

SIR was calculated from pre-fault and fault voltage magnitude as SIR = 206.667/38.59 -1= 4.35

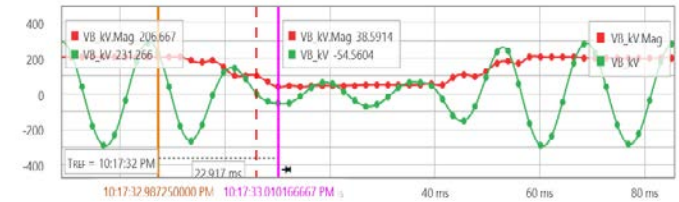


Figure-14: Remote end B-G fault

There was no delay added to account for CVT transients. The relay was tested, adding a one cycle delay, and relay did not operate.

Case Study-2:345 kV Phase to Phase at the remote end:

At a 345 KV substation, a wave trap burned open and resulted in a phase to phase fault.

At one of the remote ends of a 20.8-mile line connected to this faulted station, the zone 1 phase distance relays in both the primary and secondary systems over tripped despite the reaches set at 83% of the line's impedance. Both relays were sub-cycle static relays of the same model and vintage. The voltage input was from an active CVT. Investigations into this operation at the time reported no system/line modeling errors, no bad in-service relays settings, and no drifting reaches found during testing of the line relays. With both zone-1 relays operating for the same remote substation fault, analysis identified CVT transient overreach as the likely cause of the over operation. From CAPE fault program, SIR was calculated to be 2.17.

The static relays have no settable zone delay. To avoiding scheme modifications to add in a delay and possible future over tripping events, the zone-1 reaches were reduced to 70% of the line's impedance.

IX. Conclusions

CVTs used to provide voltage input to distance relay generate transient for one to two cycles after a disturbance due to stored energy in capacitance. In systems with high source to line impedance ratios, CVT transients may dominate during the transient period and if measurements and decisions are made within this transient period, they are prone to errors. The error in measurement of the impedance reach seems to be influenced by the capacitance values of CVTs and on the type of ferro-resonance suppression filters installed in CVTs. CVT designs with lower capacitance values and with active ferro-resonance suppression filters tend to generate transients affecting measurement resulting in overreach of zone 1 elements.

Use of new class of CVTs, type T3, seem to install damping device to reduce the errors to less than 2% in half a cycle or 4% in one cycle after the fault incidence. It is also highly recommended to request test reports from CVT manufacturers at various loading to determine errors and duration to aid decision on the Zone-1reach and on the delay if required.

Relay logic implemented in modern relays tend to minimize the overreach by adding delays at high SIR based on impedance measurement, voltage and current thresholds.

Use of full secondary voltage instead of tapped value is suggested to improve the signal to noise ratio for the voltage signal.

Detailed testing for a specific location with highest SIR encountered would be the best way to determine the relay performance.

On systems determined to have high SIR, intentional delays or/and reduction in zone 1 reach may be necessary to prevent operations beyond the protected line section.

X. References

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